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[54] **INSULATED GATE BIPOLAR TRANSISTOR PROVIDED WITH A MINORITY CARRIER EXTRACTING LAYER**

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Related U.S. Application Data

[63] Continuation of Ser. No. 276,486, Jul. 18, 1994, abandoned, which is a continuation of Ser. No. 937,161, Aug. 31, 1992, abandoned, which is a division of Ser. No. 710,721, Jun. 7, 1991, Pat. No. 5,169,793.

[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.** **257/139**; 257/786

[58] **Field of Search** 257/139, 786

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[57] **ABSTRACT**

A p type pad well layer is formed at the surface of an n^- type drain layer under a gate bonding pad and the surface thereof is provided with a p^{++} type pad layer to be provided with lower resistivity. The p^{++} type pad layer is connected with a source electrode through a contact hole. Since the gate electrode supplying each cell with gate potential is of a pattern having extensions in a comb-teeth form arranged along the boundary between the pad region and the cell region, there is present substantially no gate electrode under the pad. Hence, introduction of impurities into the entire surface of the well layer under the pad region can be performed simultaneously with formation of p^{++} type contact layers after the formation of the gate electrode, and accordingly, the low resistance p^{++} type pad layer can be easily formed. The p^{++} type pad layer serves as a low resistance path for allowing the holes flowing into the region under the pad region of the insulated gate bipolar transistor to escape to the source electrode, whereby occurrence of the latch up and increase in the turn-off time due to the minority carriers concentrating into the border portion cell located adjacent to the pad region can be prevented.

10 Claims, 16 Drawing Sheets